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STACKED VIA WITH SPECIALLY DESIGNED LANDING PAD FOR INTEGRATED SEMICONDUCTOR STRUCTURES

Cross-Reference to Related Application:

This application is a continuation of copending International Application No. PCT/DE00/02864, filed August 23, 2000, which designated the United States.

Background of the Invention:

Field of the Invention:

The invention lies in the semiconductor technology field. More specifically, the invention relates to an integrated semiconductor structure having at least one contact which extends through a plurality of layers and serves for electrically contact-connecting regions of the semiconductor structure. The contact has a first contact hole filling in a first layer and a second contact hole filling in a second layer and, in an intermediate layer situated between the first and second layers, an intermediate structure for connecting the first contact hole filling to the second contact hole filling.

Such contacts introduced into layer sequences of this type are referred to as a stacked vias. A stacked via serves to

electrically connect a regions buried below such structures through the overlying layer sequence. In multilayer metallizations, in particular, the contacts have to be led through the individual metal layers and the insulating oxide layers situated in between. To that end, after the deposition of each plane, a lithographically formed opening (via) is etched free and then filled with a conductive material. In the metal planes situated between the oxide layers, metal islands are produced likewise by lithography. These metal islands referred to as landing pads serve for electrically connecting the via introduced in the underlying oxide layer to the via that is to be introduced above it in the next oxide layer to be deposited.

The contact sequences comprising vias and landing pads fabricated in this way are susceptible, on account of their lithographic mode of fabrication, to incorrect settings primarily during the mask exposure. Principally an incorrect setting of the stepper, a defocusing, an incorrect exposure dose and the distance of outer structures from the optical axis of the mask exposure, the distance having different values depending on the exposure field size, lead to the effect known as line shortening, wherein structural elements are imaged too small and e.g. lines are imaged too short. For this reason, the metal islands for via contact-connection are dimensioned to be larger than is actually necessary, in order

that the stacked via nonetheless electrically conducts even in the case of vias not lying exactly one above the other or in the case of a lateral offset or excessively small dimensions of the metal island.

In the design of the course of metallization tracks in the metal plane, a periodic basic grid made of points or lines which are arranged in accordance with the edges or corners of a square is generally taken as a basis. On this basic grid, the metal islands, which are intended to conduct only in the vertical direction perpendicular to the metallization plane, are marked as a square that is as small as possible, in order that it maintains the largest possible distance from adjacent points of the basic grid. In view of the line shortening, however, which is critical in both dimensions in the case of the square metal island, narrow limits are imposed on the possible reduction of the contact size. In practice, landing pads are subsequently enlarged again after the conclusion of the layout design. However, at the latest when the design, once developed, is reduced in size by a certain shrink factor, the limit is rapidly reached at which the minimum distance from adjacent metal tracks which is prescribed by the design rules is undershot or the reliable contact-connection of vias lying one above the other is no longer ensured.

A further disadvantage is that resist structures for the production of conventional landing pads can become detached from the support. As a result of focus fluctuations that increase with the substrate area, resist structures with obliquely inclined side walls are produced. Particularly resist structures with an upwardly increasing cross-sectional area are easily detached from the metallization layer during spinning off and spread over the substrate.

Summary of the Invention:

It is accordingly an object of the invention to provide an integrated semiconductor structure, which overcomes the above-mentioned disadvantages of the heretofore-known devices and methods of this general type and which ensures that electrical contacts extending through a plurality of layers conduct electrically with sufficient security against faults despite increasing miniaturization; this is to be ensured without lateral distances prescribed by design rules being undershot. Furthermore, it is an object of the present invention to provide a semiconductor structure of this type which, on account of its structure, can be fabricated without the above-described postprocessing in the form of subsequent expansion of landing pads. Finally, the intention is that the semiconductor structure to be produced can be fabricated with a lower risk of resist structures chipping off during the spinning off process.

With the foregoing and other objects in view there is provided, in accordance with the invention, an integrated semiconductor structure having a plurality of layers, a contact structure extending through a plurality of layers and serving for electrically contact-connecting regions of the semiconductor structure. The contact structure comprises a first contact hole filling in a first layer, a second contact hole filling in a second layer, and an intermediate structure in an intermediate layer disposed between the first layer and the second layer and connecting the first contact hole filling with the second contact hole filling, the intermediate structure forming an interconnect having a length between longitudinal ends thereof and a given width, and a contact area at each of the longitudinal ends with a contact area width greater than the given width.

In other words, the intermediate structure has an interconnect running in the intermediate layer, and the interconnect is formed with end areas that are wider than the connecting structure in between.

The invention exploits the fact that the line shortening effect is less pronounced in the case of a line than in the case of a small, almost point-like contact area. Therefore, on the basis of the basic grid used, a line rather than a point

is selected as the basic pattern for a contact area, so that rather than two points, a point and a line meet at the connection between via and landing pad. According to the invention, the contact hole fillings in the oxide layers, above and below the metallization plane, considered from the plan view, are arranged laterally offset relative to one another. The semiconductor structures provided with the landing pads formed according to the invention are shrinkable to a degree at which conventional square metal contacts are no longer suitable for production. Since the line shortening has a less pronounced effect on the metal island formed as an interconnect, the postprocessing conventionally used after the conclusion of the layout design can be obviated. The invention furthermore has the advantage that a plurality of stacked vias running next to one another can run closely next to one another, namely at a distance of a respective length of the basic grid in each plane, whereas conventional square and subsequently expanded metal contacts, on account of design rule contraventions, had to run at a distance of two basic lengths from one another or from further metallization tracks. As a result, despite the originally point-type contacts being enlarged to form interconnects, there is an increase in the shrink factor of the entire structure.

In accordance with a preferred embodiment of the invention, the interconnect connects two nearest points of a periodic basic grid to one another.

In accordance with an additional feature of the invention, the intermediate structure has a square contact area at each end of the interconnect. Even with differently shaped contact areas at both ends of the interconnect, the result is that the shape of the intermediate structure or metal island has an approximately bone-like appearance.

The metal island is expediently composed of the same conductive material of which the metallization plane is also composed. The vias in the adjacent, preferably oxidic layers preferably predominantly contain tungsten.

A development of the invention which is directed at multilayer metallizations provides for at least one further metallization layer to be adjacent to the first and/or the second layer.

Any semiconductor structures, but preferably DRAMs, in particular embedded DRAMs, are appropriate as integrated semiconductor structures with the stacked vias configured according to the invention.

Other features which are considered as characteristic for the invention are set forth in the appended claims.

Although the invention is illustrated and described herein as embodied in a stacked via with specially designed landing pad for integrated semiconductor structures, it is nevertheless not intended to be limited to the details shown, since various modifications and structural changes may be made therein without departing from the spirit of the invention and within the scope and range of equivalents of the claims.

The construction and method of operation of the invention, however, together with additional objects and advantages thereof will be best understood from the following description of specific embodiments when read in connection with the accompanying drawings.

Brief Description of the Drawings:

Fig. 1 is a diagrammatic sectional view of a model of a stacked via formed in a prior art process before layout postprocessing;

Fig. 2 is a plan view onto the metallization island in the stacked via of Fig. 1 before and after layout postprocessing; and

Fig. 3 is a plan view onto a metallization island formed in accordance with the invention.

Description of the Preferred Embodiments:

Referring now to the figures of the drawing in detail and first, particularly, to Fig. 1 thereof, there is shown a conventional square landing pad that extends around an edge of width o on all four sides beyond the dimensions b at the bottom of a via. The landing pad which, with a dimension of $l = b + 2o$, maintains sufficient distances from adjacent metallization tracks and therefore conforms to design rules is enlarged in the context of the layout postprocessing in accordance with Fig. 2.

With this size, although the vertically adjacent vias are contact-connected, there is nonetheless the fear of short circuits arising within the metallization plane.

Fig. 3 shows a landing pad according to the invention in the shape of a bone or a dumbbell (or an H), formed from an interconnect having a width w and a length s+l, strengthened at both ends by square end contacts having the dimension l. Unlike those in Fig. 2, these squares are no longer enlarged. For this reason, the bone structure illustrated, even though it occupies two points of the basic grid, fits better into the grid layout and, even in the case of subsequent

miniaturization of the circuit, carries a more reliable via contact-connection than the expanded square metal island illustrated on the right in Fig. 2.

It goes without saying that it lies within the scope of the present invention for the form of the metal contact according to the invention to be altered, extended, or adapted to an altered basic grid. Thus, by way of example, it is possible for a vertically running interconnect with terminating square contact area to be added to the bone shape illustrated in Fig. 3. In this case, too, the landing pad occupies only two adjacent points of the basic grid in each dimension, whereas a conventionally configured square landing pad enlarged by postprocessing exceeds the minimum distances from the adjacent point of the basic grid in each direction and therefore effectively takes up a basic area of 3 times 3 grid points.